IN THE CLAIMS

Please cancel claims 12 and 22 without prejudice or disclaimer.

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claims 1-7 (canceled)

Claim 8 (original) A register file comprising:

a first plurality of cells coupled to a first local bit line;

a global bit line;

a first tri-state inverter coupled between the first local bit line and the global bit line, the first tri-state inverter controlled by a first local select signal;

a second plurality of cells coupled to a second local bit line;

a second tri-state inverter coupled between the second local bit line and the global bit line, the second tri-state inverter controlled by a second local select signal;

a latch with its input coupled to the global bit line; and

a third tri-state inverter coupled between an output of the latch and the global bit line, the third tri-state inverter controlled by a hold signal.

Claim 9 (original) The register file as recited in claim 8, further comprising:

an inverter coupled between the global bit line and the input of the latch.

Claim 10 (original) The register file as recited in claim 8, wherein when the third tri-state inverter is activated, the first and second local select signals are deactivated.

Claims 11-17 (canceled)

Claim 18 (original) A register file comprising:

a first plurality of cells coupled to a first local bit line;

a global bit line;

a first transmission gate coupled between the first local bit line and the global bit line, the first transmission gate controlled by a first local select signal;

a second plurality of cells coupled to a second local bit line;

a second transmission gate coupled between the second local bit line and the global bit line, the second transmission gate controlled by a second local select signal;

a latch with its input coupled to the global bit line; and

a third transmission gate coupled between an output of the latch and the global bit line, the third transmission gate controlled by a hold signal.

Claim 19 (original) The register file as recited in claim 8, further comprising:

an inverter coupled between the global bit line and the input of the latch.

Claim 20 (original) The register file as recited in claim 8, wherein when the third transmission gate is activated, the first and second local select signals are deactivated.

Claims 21-25 (canceled)